



PolyCore Software

Simplifying Multicore

Virtual Development Platform for Many-MultiCore Applications

By

Ted Gribb

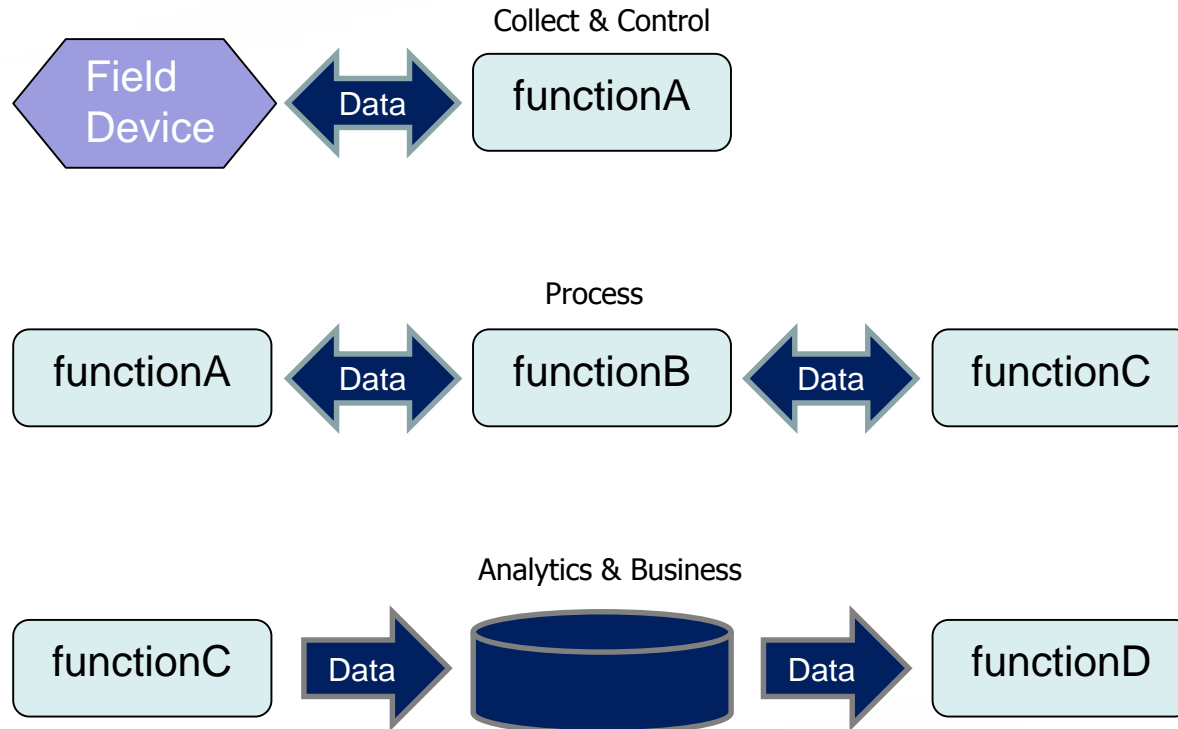
PolyCore Software, Inc

www.PolyCoreSoftware.com



Data Sharing

Heart of Computing

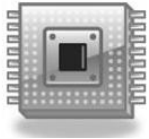




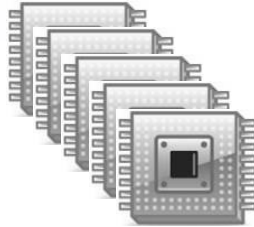
Data Sharing

Distributing the Load

Single Core

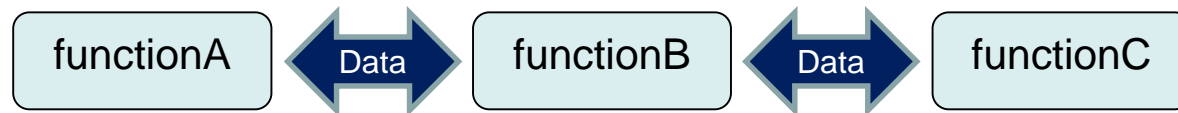


Multi-Core



Microcontroller
General Purpose Computer
DSP
FPGA
Special Function

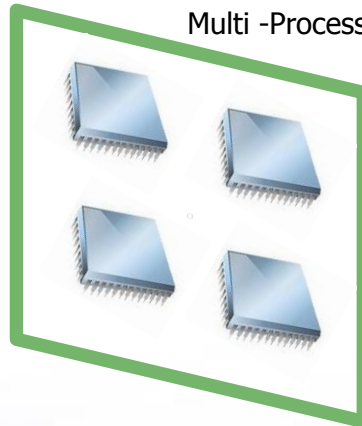
Process



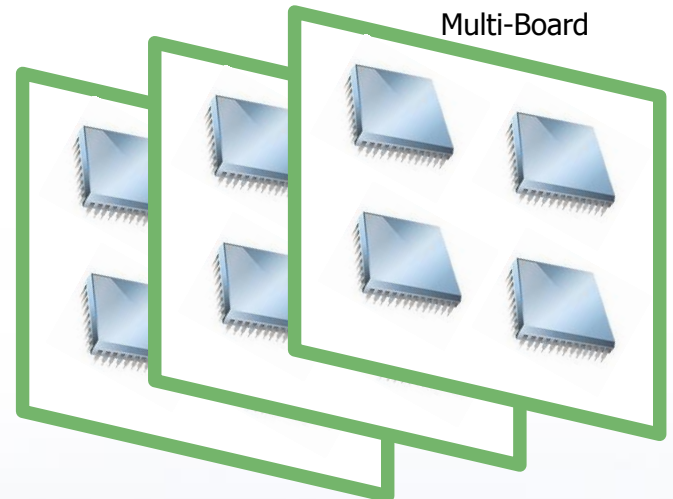
Single Processor



Multi -Processor

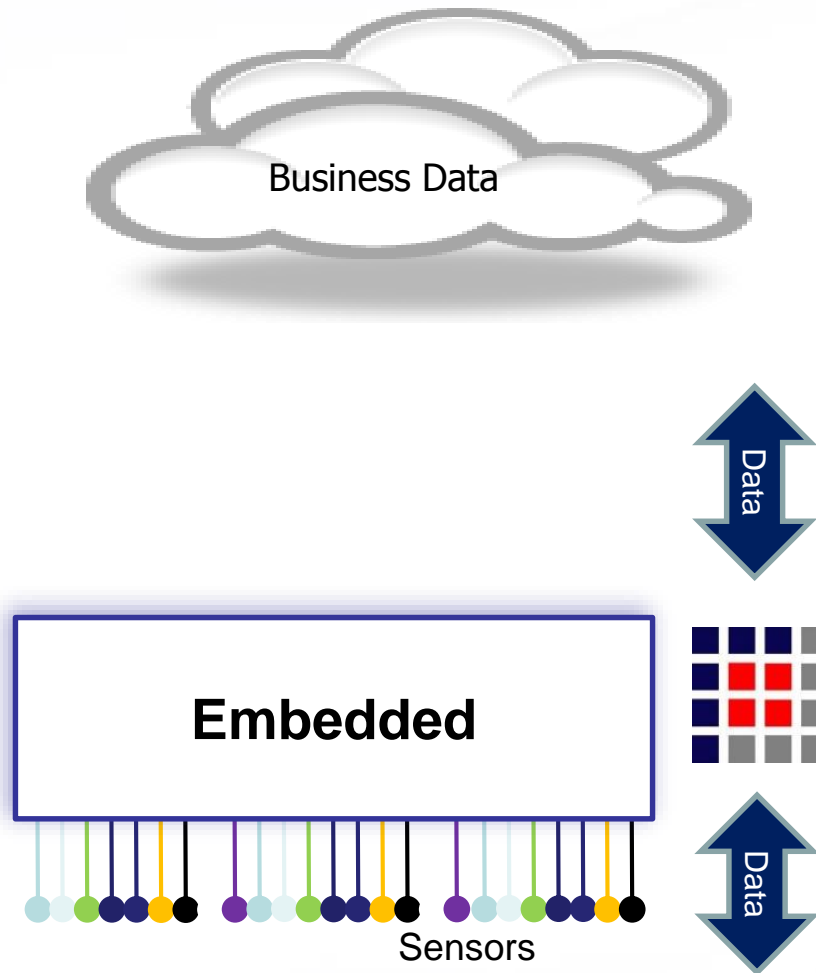


Multi-Board





IoT: Data Sharing



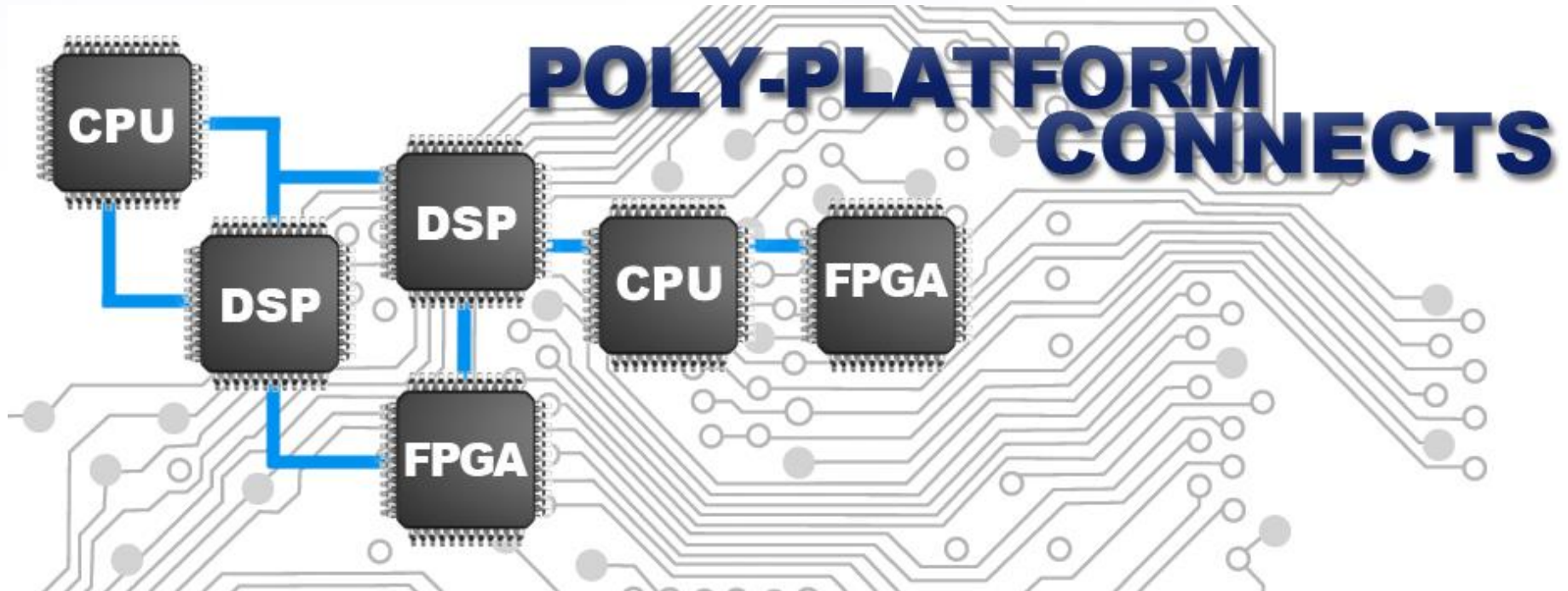
Poly-Platform

Unifies Communication:

- Normalizes Data Sharing
- Same API to any destination
 - MCAPI
 - Application Portability
- Data Integrity
- Support for:
 - Core Type
 - OSES
 - Transports



PolyCore Software Connects Applications



Many Multi-(s)

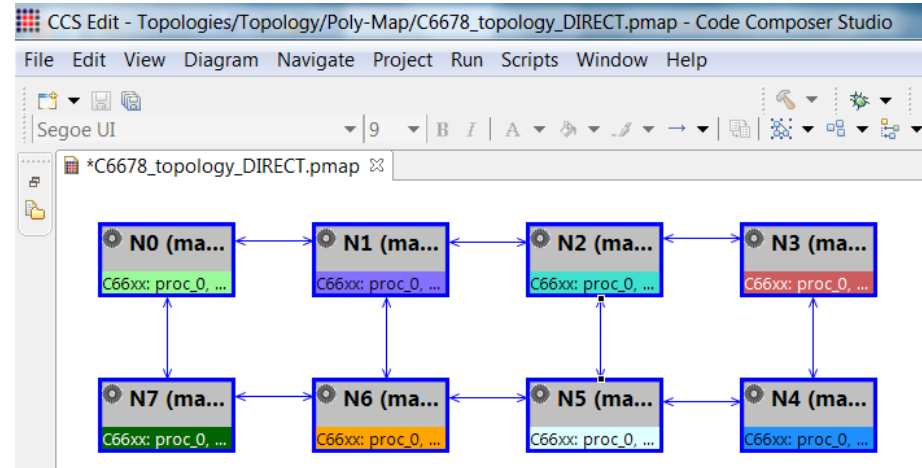
- Cores per chip/board/system
- Accelerators
- Operating Systems (Linux, Windows, RTOS)
- Transports (on-chip, wire)
- Memory Architectures



Poly-Platform

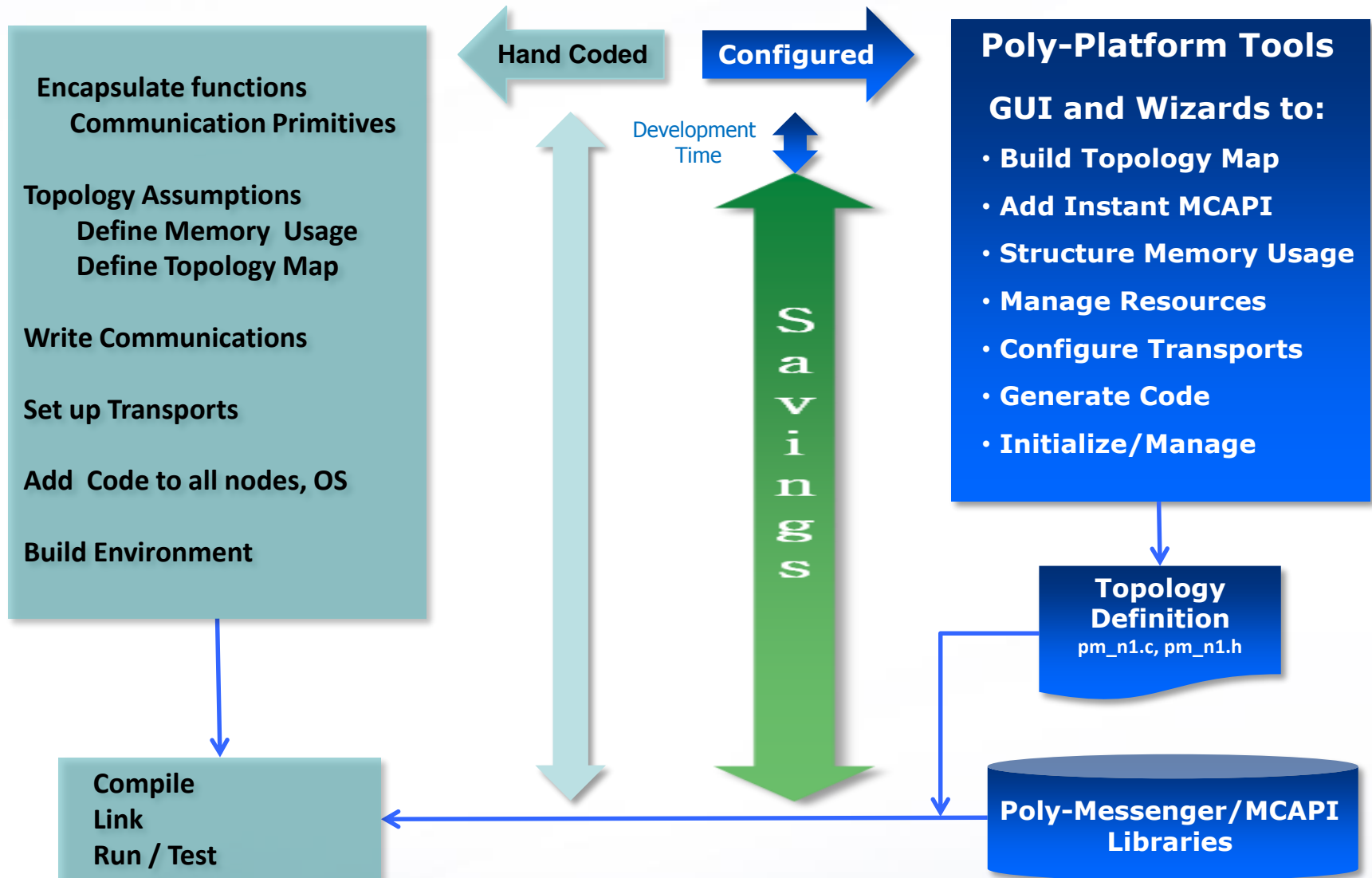
Productivity Development Tools and Runtime for data sharing and synchronization

- Message Passing
 - Unlimited Scalability
 - Synchronizing
- Standards
 - MCAPAPI support
 - Eclipse
- Virtualizes Platform
 - SMP and AMP
 - Heterogeneous and Homogenous
 - CPU, OS, Transports, Memory
 - Hardware Accelerators
- Code generated from Poly-Maps





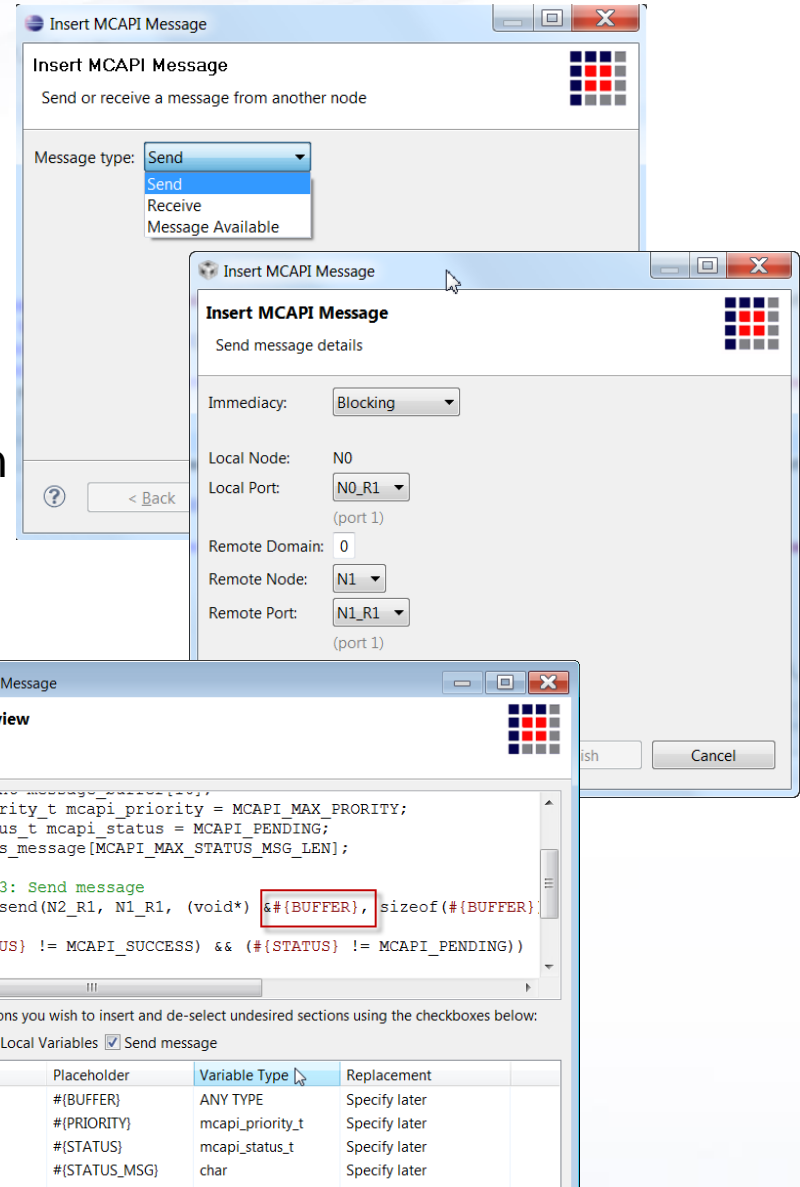
Poly-Platform™ Programming Model Benefit





Poly-Platform: Add MCAPI Primitives

- Add MCAPI to Application
- Guides Developer w/ Wizards
 - Little to no MCAPI knowledge
 - MCAPI code Template
 - Insert MCAPI calls into the application
 - All MCAPI functions are available
- Improves Development Time
- Improves Code Quality
 - Uses Poly-Maps
 - Known Nodes
 - Validates Types



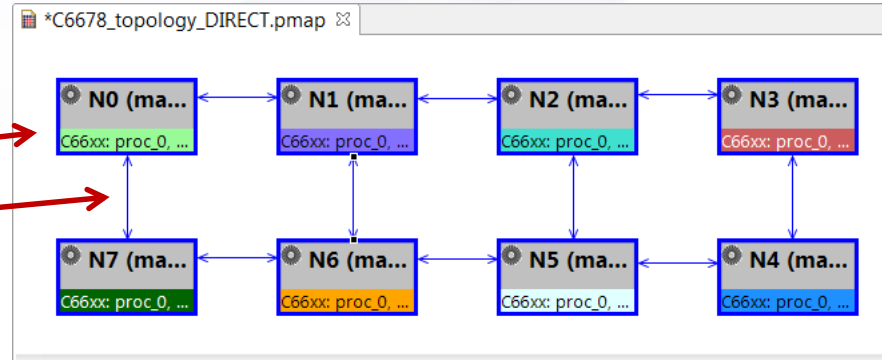


Poly-Platform: Define/Configure Topology

- Configure vs. Program

- Draw

- Nodes
 - Transports



- Define Node

- Properties
 - Processor
 - Core #
 - Operating System

N7

Node

Repositories

Accessible Regions

Related Pools

Node Properties

Operating System: DSPBIOS

Processor: proc_0 - C66xx (8 cores)

Core ID: 7

Master: ☒

Domain: 0

Comment:

- Transport to use

- Shared Memory/DMA
 - SRIO
 - TCP/IP
 - Infiniband
 - Serial/USB
 - Other

Console Properties

Link from N2 to N1 (TIC66SMDMA LinkDriver)

Link Edit Parameters of Link from N2 to N1

Source Node Parameters (N2)

Name	Value	Type
OutRemoteCoreId	0	out
OutSharedMemAddr	0x00800000	out
OutDMATriggerSize	1	out
OutGateId	L_21	out
InRemoteCoreId	0	in
InSharedMemAddr	0x00800000	in
InGateId	L_12	in
InQueueBufBase	0x00800000	in
InQueueHdrBase	0	in
InNumQueueBufs	5	in
InBufferSize	2048	in

Link Driver: TIC66SMDMA LinkDriver

Link Subnet: NET1

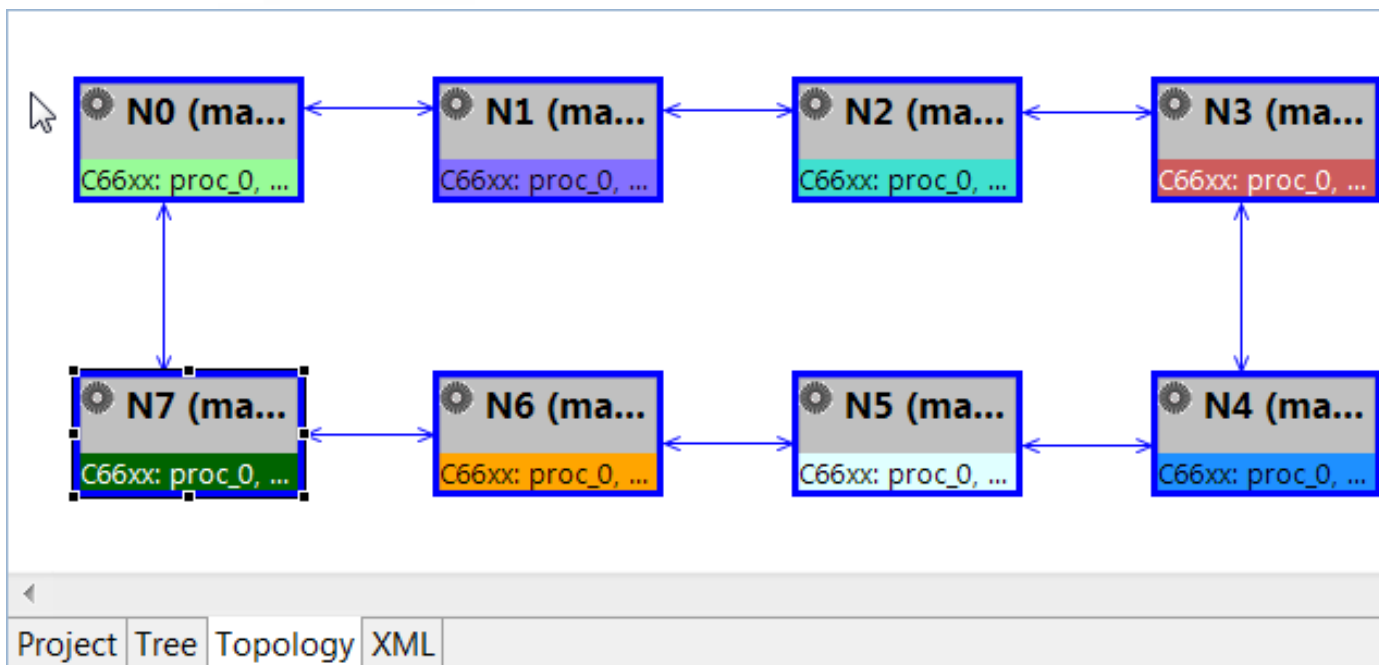
Link Direction: Bidirectional

Apply Changes

- Quickly Define & Try



Map Application to Platform





Configure Transports

- Shared Memory – DMA support

Console Properties

Link from N2 to N1 (TIC66SMDMALinkDriver)

Link Edit Parameters of Link from N2 to N1

Source Node Parameters (N2)

Name	Value	Type
← OutRemoteCoreId	0	out
← OutSharedMemAddr	0x00800000	out
← OutDMATriggerSize	1	out
← OutGateId	L_21	out
→ InRemoteCoreId	0	in
→ InSharedMemAddr	0x00800000	in
→ InGateId	L_12	in
→ InQueueBufBase	0x00800000	in
→ InQueueHdrBase	0	in
→ InNumQueueBufs	5	in
→ InBufferSize	2048	in

Link Driver: TIC66SMDMALinkDriver

Link Subnet: NET1

Link Direction: Bidirectional

Apply Changes

- sRIO

Console Properties

Link from N1 to N2 (TISRIOLinkDriver)

Link Edit Parameters of Link from N1 to N2

Source Node Parameters (N1)

Name	Value	Type
← OutSRIOSocketType	9	out
← OutMySRIOAddress1	0xBEEF	out
← OutMySRIOAddress2	1	out
← OutMySRIOAddress3	1	out
← OutMySRIOAddress4	0	out
← OutToSRIOAddress1	0x4560	out
← OutToSRIOAddress2	2	out
← OutToSRIOAddress3	4	out
← OutToSRIOAddress4	0	out
→ InSRIOSocketType	9	in
→ InMySRIOAddress1	0xBEEF	in
→ InMySRIOAddress2	1	in
→ InMySRIOAddress3	2	in
→ InMySRIOAddress4	0	in

Link Driver: TISRIOLinkDriver

Link Subnet: NET1

Link Direction: Bidirectional

Apply Changes



Configure Processor

- Topology

The screenshot displays the PolyCore configuration interface. On the left, a topology diagram shows three nodes: N7 (ma...), N6 (ma...), and N5 (ma...), each labeled with 'C66xx: proc_0, ...'. Below the diagram, the 'Node Properties' for node N7 are shown. The 'Node' section includes 'Repositories', 'Accessible Regions', and 'Related Pools'. The 'Node Properties' section includes 'Operating System' (DSPBIOS), 'Processor' (proc_0 - C66xx (8 cores)), 'Core ID' (7), 'Master' (checked), 'Domain' (0), and 'Comment'.

On the right, the 'Poly-Mapper' window is open, showing a project tree for 'C6678_topology_direct.pmap'. The tree includes 'platform:/resource/Topologies/Topology/Poly-Map/C6678_topology_direct.pmap', 'Project C6678_topology', 'Priority Level HIGH', 'Priority Level LOW', 'Max Payload Size 2048', 'Processor proc_0 (C66xx)', 'Subnet NET1', 'Combined Pool CMB1 (MAR1)', and 'Message Queue Pool MQP1 (MAR1)'. Below the tree, the 'Edit Combined Pool' window is open, showing a table of properties for 'Combined Pool CMB1 (MAR1)'.

Property	Value
Header	With_Header
Name	CMB1
Management	Software
Initializing Node	N0
Memory Region	MAR1

At the bottom of the 'Edit Combined Pool' window, there are fields for 'Waiter Pool' (Waiter Pool: WT1), 'Data Buffer Size' (2048), and 'Number of Sub-pools' (4).




Poly-Platform: Memory Maps

Create, Edit, Validate

- Configure vs. Program
- Single core or multicore
- Validates size and alignment
- Simplifies memory organization
- Helps avoid memory overlaps
- Enhances Portability

Poly-Mapper - Memory Map Editor (Full Mode)

 Main Settings

Memory Map Name Description Number of cores

Export Directory Default Alignment

Constants & Sections

Constants

Name: Information: Default Alignment: Permissions:

Scope: Type: Global Start: Local Start: Size:

View: ☐ Local ☒ Global

Range Name	Fixed	Reserved	Start Address	End Address	Size	Alignment	Type	Details
poolMem1			0x62800000	0x628027FF	10240	128	...	
poolMem2			0x62802800	0x62804FFF	10240	128	...	
heap1	✓		0x62805000	0x6280CFFF	32768	128	...	
heap2	✓		0x6280D000	0x6281CFFF	65536	128	...	
System		✓	0x6281D000	0x6283CFFF	131072	128	...	

Address Name	Reserved	Start Address	Type	Details
Flag1		0x62810000		...



PolyCore Software – *Simplifying Multicore™*

Poly-Platform: Development Framework for Multicore Applications

- Preserves Software Investment
 - Scales & Abstraction
 - Homogeneous/heterogeneous environments
- Improves Development Time/Costs
 - Quickly start on sophisticated platforms
 - Rapid (re)configuration to test
 - Recurring
- Performance: Optimal use of compute resources
- Enhanced Code Quality generated from the Configuration
 - Consistent & repeatable across platforms



Build for today's architecture ...And reuse on tomorrow's



Thank you

PolyCore Software
+1 650.570.5942

www.PolyCoreSoftware.com

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