SiFive

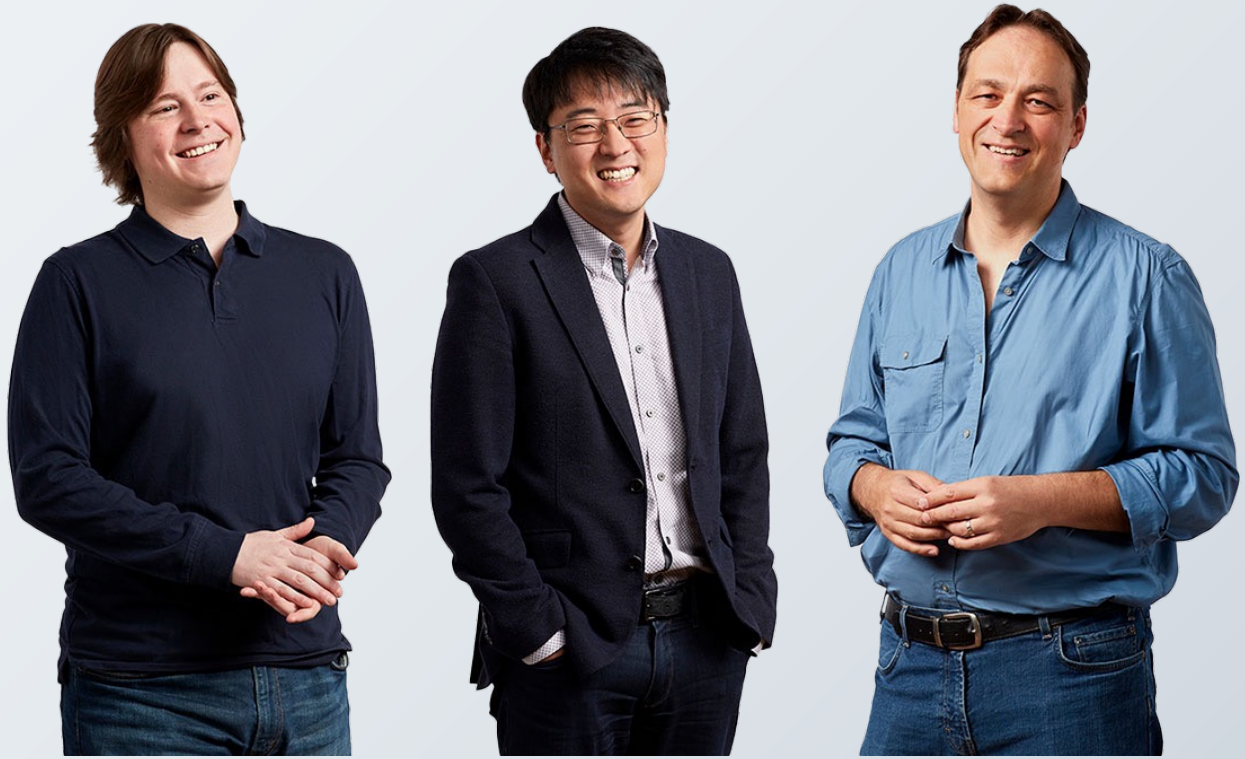
SiFive/RISC-V Overview

Multi Core High performance computing

Sam Rogan, Yoshihito Kondo
SiFive Japan K.K.

Nov 16th , 2023

Founded by the inventors of RISC-V



- SiFive is the RISC-V founder & brand standard
- Leading the commercialization effort since 2010
- World's largest technology work with SiFive to adopt RISC-V
- Largest team & investment
- Recognized as the Most Respected Private Semiconductor Company
- 2018, 2019, 2020, 2022

RISC-V International

SiFive

Disruptive **Technology**

Barriers	Legacy ISA	RISC-V ISA
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions, open and proprietary cores
Software ecosystem	Extensive	Growing rapidly

RISC-V®

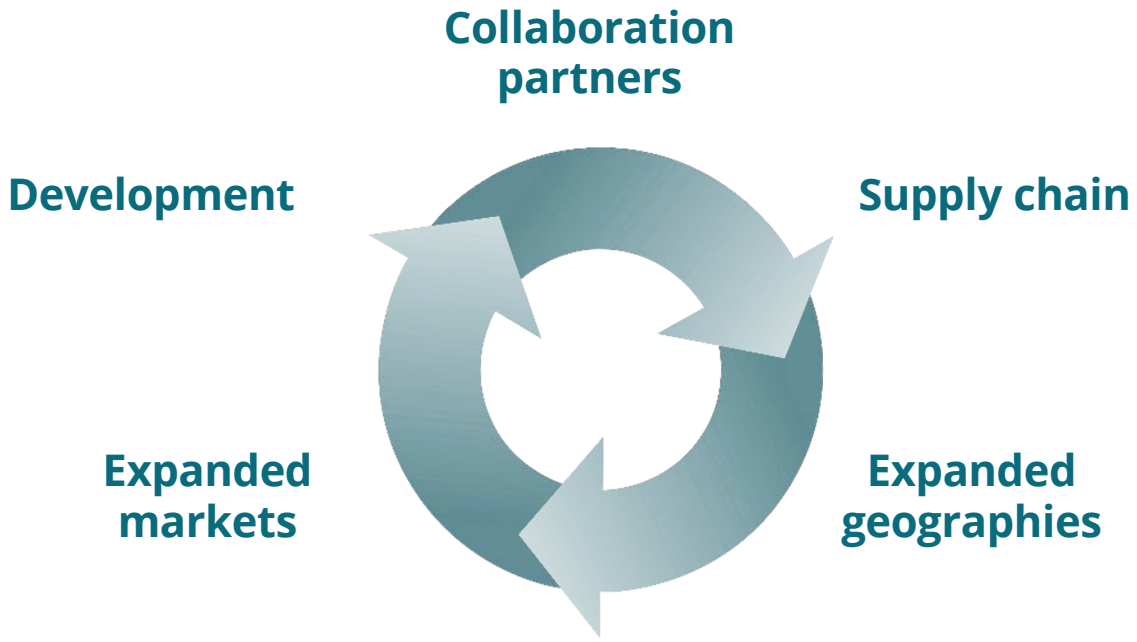
SiFive

Unconstrained **Opportunity**

Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

RISC-V Business Model

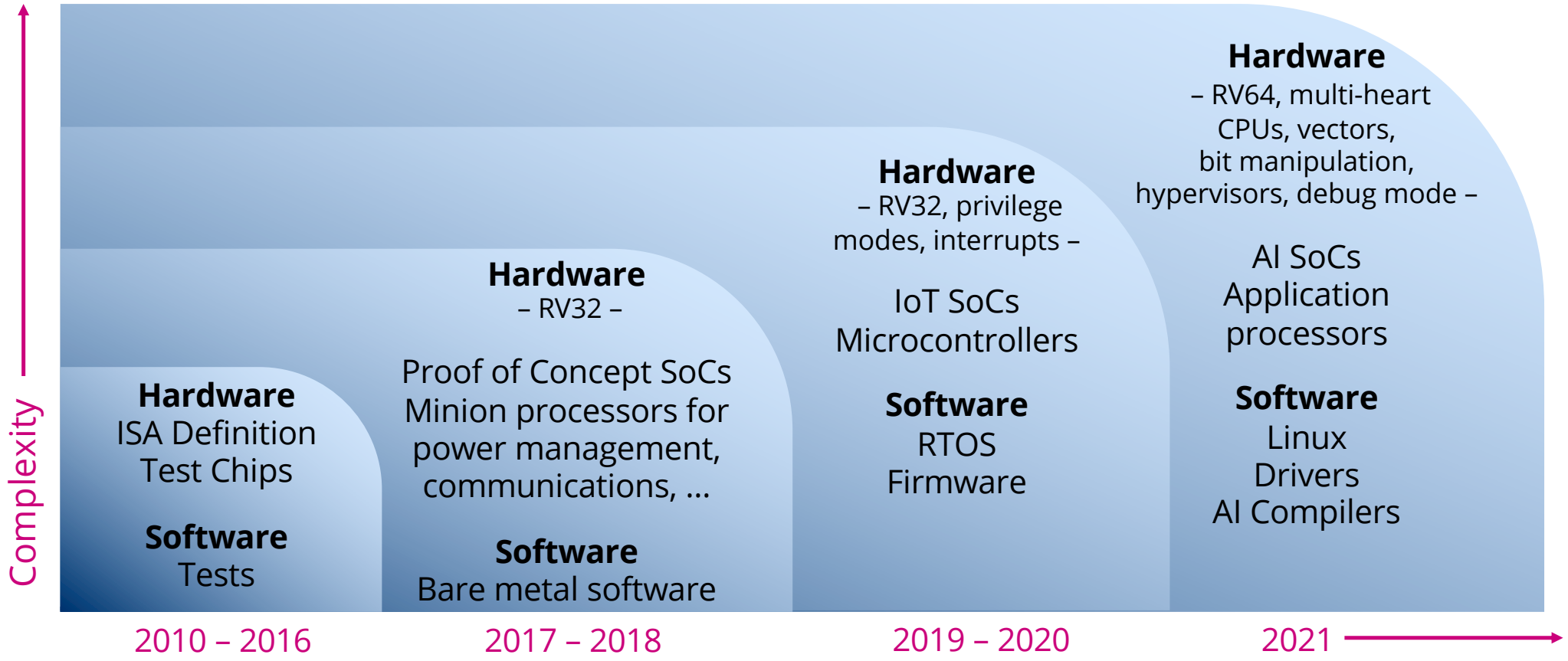


RISC-V®

RISC-V International

SiFive

Industry innovation on RISC-V



RISC-V®

The Rise of RISC-V

Over 80 billion RISC-V cores projected to ship by 2025

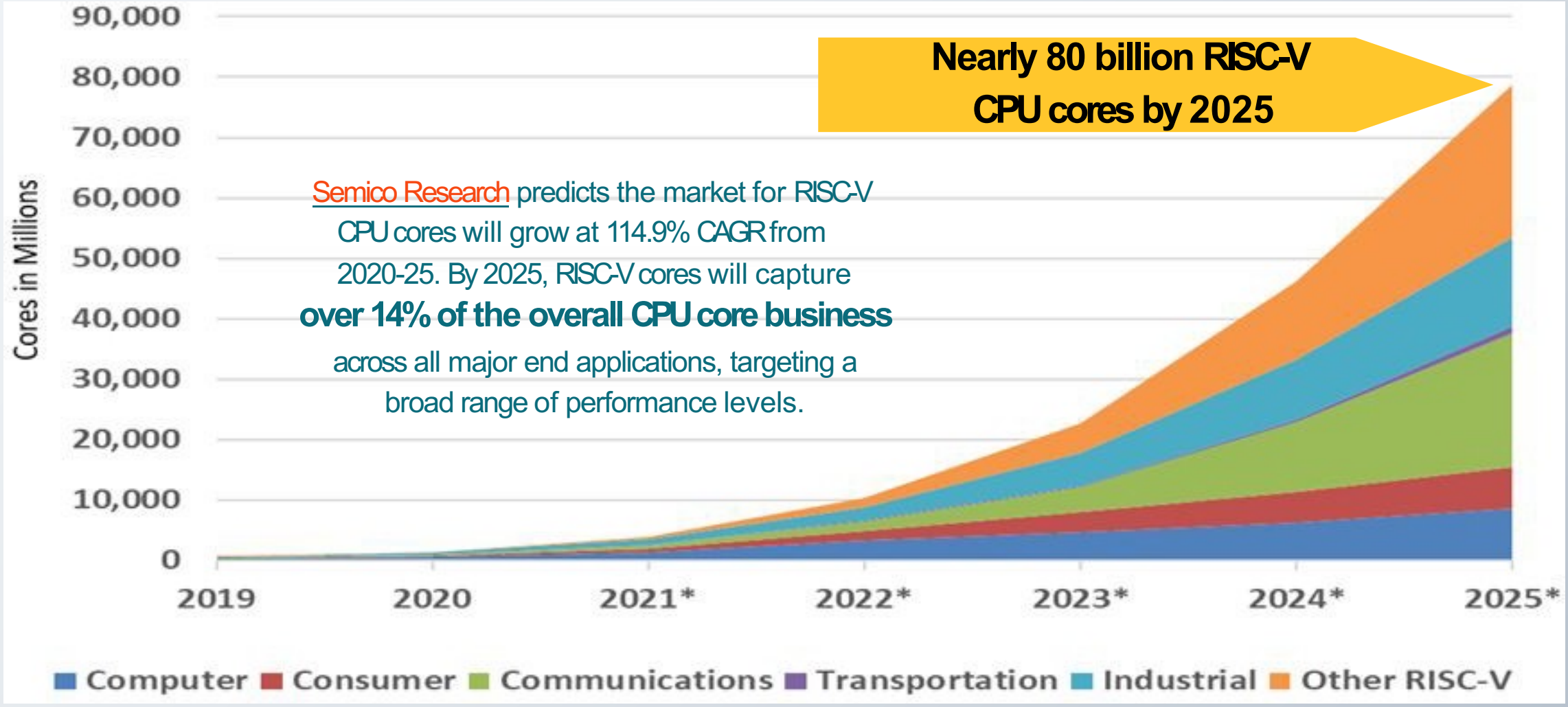
Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of ***80 billion RISC-V cores by 2025***

SoCs shipping with RISC-V between 2020 and 2025 projects ***114.9% CAGR***

Source: Semico Research

Over 3,800 RISC-V International members across 70 countries

Rapid RISC-V growth led by industrial



Source: Semico Research Corp, March 2021

RISC-V International now > more than 3,800 members
70 countries

RISC-V

Free, open, extensible ISA for all computing devices

SiFive

350+

Design wins

100+

Customers

8 of 10

Top semiconductor companies work with us

600+

Employees

$2.5+B

Valuation

RISC-V is Inevitable

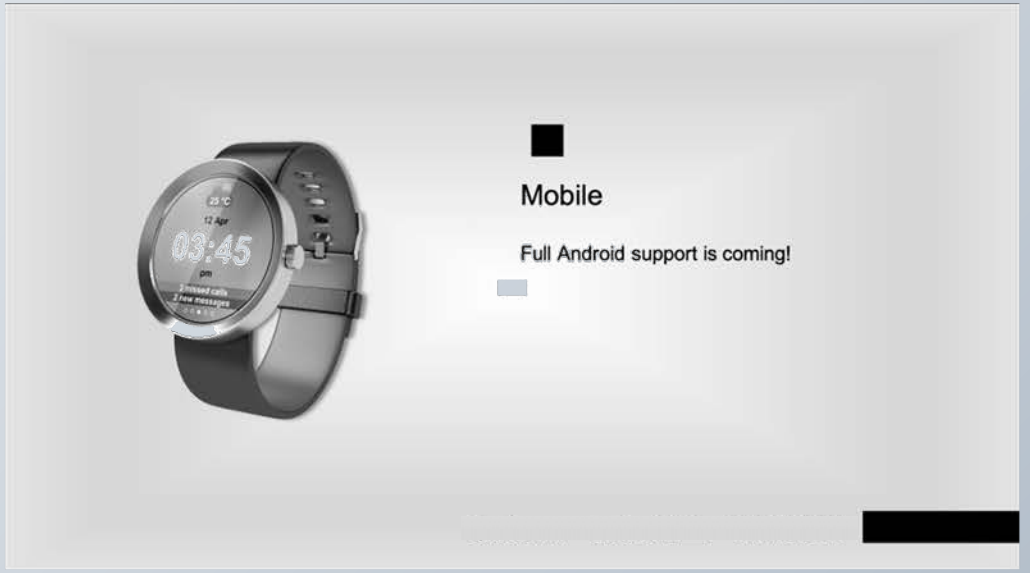
The ecosystem of the **Future** is already being deployed

- The only major global compute platform on an open standard
- Used by all top semiconductor companies
- Supported by 3800+ members in RISC-V International
- Platform of choice in China & India
- Selected by US Govt
- Taught in all Top Universities
- Publicly embraced by Intel
- The strongest, most robust ecosystem is built on open standards with multiple participants

Legacy ‘efficiency processors’ are failing the industry

- Latest market requirements are not being met by current suppliers
- No innovation for the last 5 years
- SiFive’s latest innovation brings significant upgrade opportunities
- Vector compute brings performance boost and power efficiency
- SiFive Performance portfolio enables greater design flexibility

Broad Vertical Coverage



Google uses SiFive RISC-V cores in AI compute nodes

- At the AI Hardware Summit in Santa Clara, September 14th, Krste Asanovic, SiFive Co-Founder and Chief Architect, took to the stage with Cliff Young, Google TPU Architect and MLPerf Co-Founder, to reveal how the latest **SiFive Intelligence™ X280** processor with the new SiFive Vector Coprocessor Interface Extension (**VCIX**) is being used as the AI Compute Host to provide flexible programming combined with the Google MXU (systolic matrix multiplier) accelerator in the **datacenter**.

Please find more detailed article in SiFive blog below.

https://www.sifive.com/blog/sifive-intelligence-x280-as-ai-compute-host-google

SiFive Product Portfolio

Four Product Families: Automotive, Essential, Intelligence, Performance

64-bit high-performance feature-rich OS capable application processors

32/64-bit real-time scalable performance deeply embedded processors

Automotive

P870-A
64-bit, High Perf Apps Processor
128b vector length
ASIL B, D and B/D
ASIL B | ASIL D | ASIL B/D

X280-A
AI acceleration instructions 512b vector length
ASIL B
ASIL B | ASIL D | ASIL B/D

S7-A
64-bit, high Perf. embedded ASIL D
ASIL D

E6-A
32-bit, balanced perf.
ASIL B, D
ASIL B | ASIL D

Intelligence

X200-Series
AI processor for Edge and Data Center ML applications
AI acceleration instructions
512b vector length

Performance

P400-Series
>8 SpecINT2k6/GHz
3-wide OoO core
128b vector length
Hypervisor ext.
Vector crypto
IOMMU & AIA
WorldGuard
RVA22

P500-Series
>8.6 SpecINT2k6/GHz
3-wide OoO core
Hypervisor ext.
WorldGuard
RVA20

P600-Series
>13 SpecINT2k6/GHz
4-wide OoO core
128b vector length
Hypervisor ext.
Vector crypto
IOMMU & AIA
WorldGuard
RVA22

P800-Series
>18 SpecINT2k6/GHz
6-wide OoO core
128b vector length
Hypervisor ext.
Vector crypto
IOMMU & AIA
WorldGuard
RV64GCBV

Essential

U6-Series
64-bit, high performance

U7-Series
64-bit, superscalar performance

S2-Series
64-bit, Area optimized

S6-Series
64-bit, power efficiency

S7-Series
64-bit, high performance, embedded

E2-Series
Smallest, most efficient

E6-Series
Balanced Perf.

E7-Series
32-bit, optimized Perf.

RISC-V is the Fastest Growing Software Ecosystem

siFive

Tools

ASHLING

Freedom Studio

iSYSTEM

iar

Green Hills SOFTWARE

LAUTERBACH DEVELOPMENT TOOLS

SEGGER The Embedded Experts

WNDRVR

Commercial Solutions

wolfSSL, PROVENRUN, codeplay, ELEKTROBIT, SGS, Solid Sands, WITTENSTEIN, RESILTECH Technologies for Resilience

Middleware, Libraries, Runtimes

OvS Open vSwitch, OpenMP, SPDK, OpenSSL, NGINX, Memcached, php, MySQL, redis, SLEEF SIMD Library for Evaluating Elementary Functions, DPDK DATA PLANE DEVELOPMENT KIT, PyTorch, docker, OpBL enAS, FFTW, OpenJDK, JS, OpenCV, TensorFlow

Non-Linux

Zephyr, NetBSD, seL4, RTEMS, VxWorks, freeRTOS, P, INTEGRITY Real-Time Operating System, FreeBSD

Android

WORK IN PROGRESS

android

Linux

yocto PROJECT, AUTOMOTIVE GRADE LINUX, ubuntu, openSUSE, OpenWrt, debian

Foundational Software

GCC, tianocore, AdaCore, LLVM COMPILER INFRASTRUCTURE, musl libc, KVM, MLIR, Virtual Open Systems, U-Boot

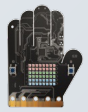
Execution Targets

HiFive1

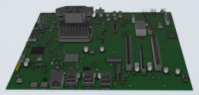
HiFive Unmatched

Microchip PolarFire Icicle

StarFive Vision Five 2



Dr. Who Inventor Kit



HiFive Pro P550

Xilinx VCU118

Digilent Arty 100T

QEMU

SPIKE

imperas

antmicro

SiFive RISC-V Embedded Software Ecosystem

SiFive

Open source solutions

Commercial solutions

SiFive RISC-V Linux Software Ecosystem

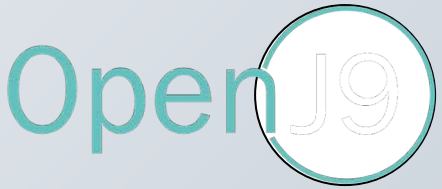
debian

fedora

ubuntu

coreboot

gentoo linux™



UNIFIED EXTENSIBLE
FIRMWARE INTERFACE

tianocore

SiFive Automotive RISC-V Ecosystem

Compilers, RTOS, Virtualization, STL, Safety consultancy…

Android is Coming!

SiFive

- Google has officially begun accepting RISC-V patches into Android Open Source Project (AOSP)
  - Keynote speech at the RISC-V summit by Google
- AOSP - Android Open Source Project
  - Upstream open-source repository for Android
  - Enables community contributions to the codebase (like adding support for RISC-V)
- Google, and others, use AOSP as the basis for their commercial OS distributions
  - Android, FireOS, WearOS, etc… all base their OS on AOSP
- Note that AOSP support does not ensure Play Store support, but this is the first hurdle to clear
  - Native Java/Flutter apps will “just work”
  - High performance applications and libraries (game engines, etc..) will still need to be ported with Android SDK

Enhancing the SiFive Performance Portfolio

Extended family of area & power efficient processors

SiFive Performance™ Family

Market **leading RISC-V** Application **Processors**

- Performance density leadership
- First with latest RISC-V features, standards, and technology
- High performance with optimized power efficiency
- SiFive momentum with NASA, Google, and Intel Horse Creek

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Intelligence

X200-Series
AI processor for Edge and Data Center ML applications
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Performance

P400-Series
>8 SpecINT2k6/GHz
3-wide OoO core
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Essential

U6-Series
64-bit, high performance

U7-Series
64-bit, superscalar performance

S2-Series
64-bit, Area optimized

S6-Series
64-bit, power efficiency

S7-Series
64-bit, high performance, embedded

E2-Series
Smallest, most efficient

E6-Series
Balanced Perf.

E7-Series
32-bit, optimized Perf.

SiFive Performance Family

2023 Product Lineup

Hypervisor extension
IOMMU & AIA
WorldGuard
RVA22

Common features

P670

>12.6 SpecINT2k6/GHz
4-wide OoO core
2x 128b VLEN RVV
Vector crypto

P650

>11.5 SpecINT2k6/GHz
4-wide OoO core

P470

>8 SpecINT2k6/GHz
3-wide OoO core
1x 128b VLEN RVV
Vector crypto

P450

>6.6 SpecINT2k6/GHz
3-wide OoO core

Home Appliance | Wearable | Feature phone | Smartphone / Premium wearable | Network appliances

SiFive Performance™ P470

Boosted
Performance

Significant upgrade to legacy efficiency cores

Small
Area

Optimized area for power constrained applications

Efficient
Power

Highly-tuned for aggressively low power consumption

Optimized
Pipeline

Out-of-Order pipeline enables optimal performance efficiency

RISC-V
Compliant

Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions

SiFive Performance™ P670

Highest
Performance

Best-in-class performance

Balanced
PPA

Optimized performance within constrained area and power envelope

Vector
Extensions

Acceleration for media, crypto and data processing

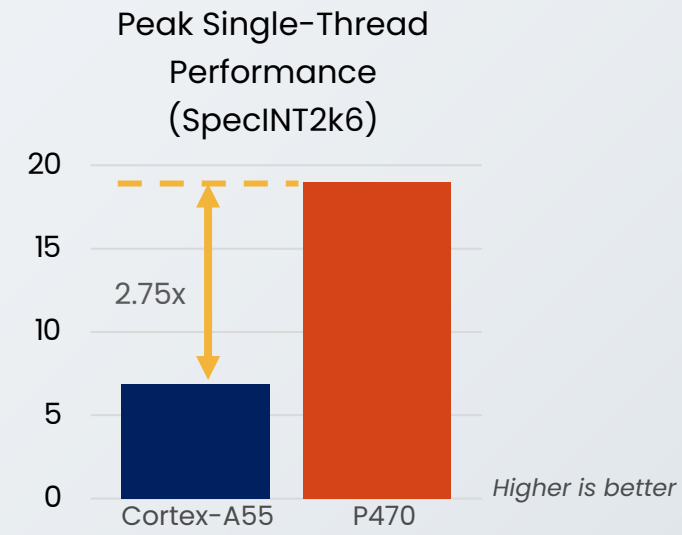
Feature
Rich

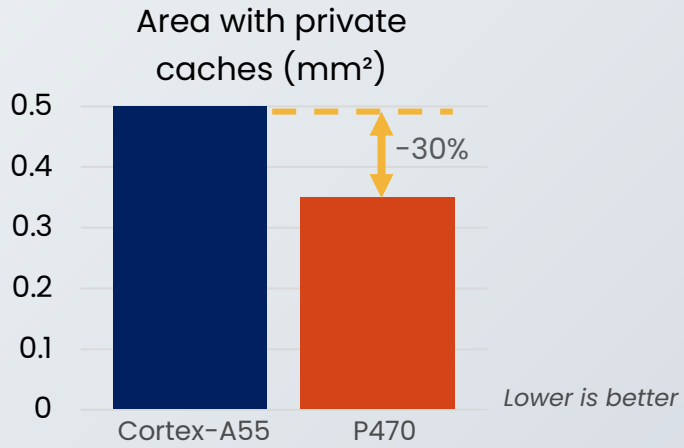
Virtualization, IOMMU, AIA, Debug & Trace, Security

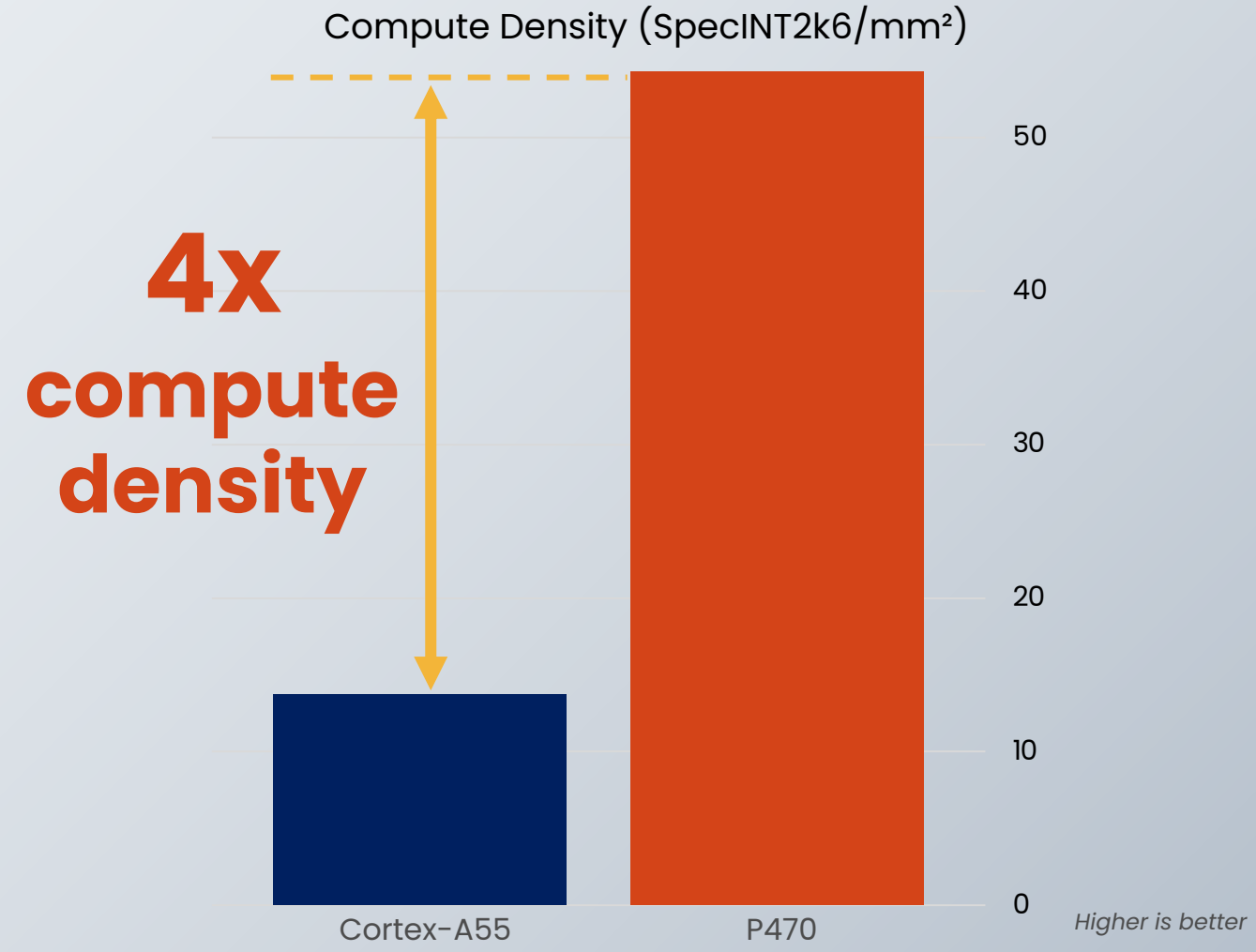
RISC-V
Compliant

Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions

P470 Peak Single-Thread Performance







*Cortex-A55: **Performance** 1.88GHz in 7nm, measured on Acer Spin 513 Chromebook with Qualcomm Snapdragon 7c. **Area**: 7nm TechInsights - Die photos show Cortex-A78 shortfall",*
*SiFive P470: **Performance** 2.97GHz in 7nm, 0.95V 32KB L1 I$ and D$, 2MB L2$. **Area**: measured in 7nm*

Upgrade to the SiFive Performance Family

Performance density leadership

High performance with optimized power efficiency

First with latest RISC-V features, standards, and technology

The P400-Series and P600-Series are available to Lead Partners in Q4 2022

SiFive

P870 High-Performance RISC-V Processor

RISC-V is based on standards

Standards Accelerate Software Adoption and Portability

Standards reduce cost

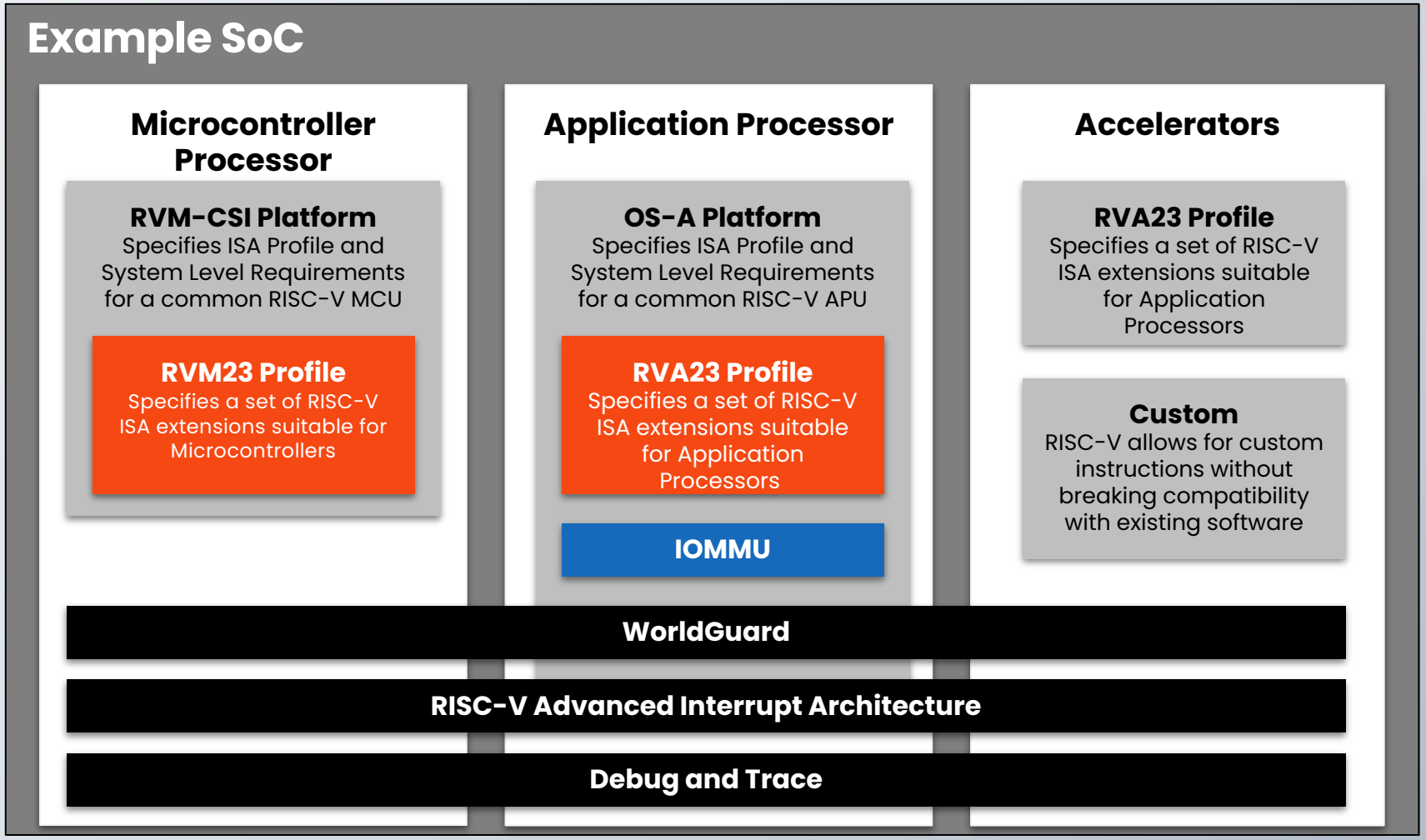
- Faster Adoption
- Compatibility across vendors

Layered standards enable customization

- RISC-V embraces customization without breaking compatibility

More than just ISA Standards

- RISC-V Standards extend beyond the Core ISA to system-level components



SiFive Performance family relentless innovation

RVA20+

P550

RVA22/RVA23

P650/P670

P450/P470

RVA23

P870

More performance
Higher core count
Leading RISC-V feature deployment

P870-A

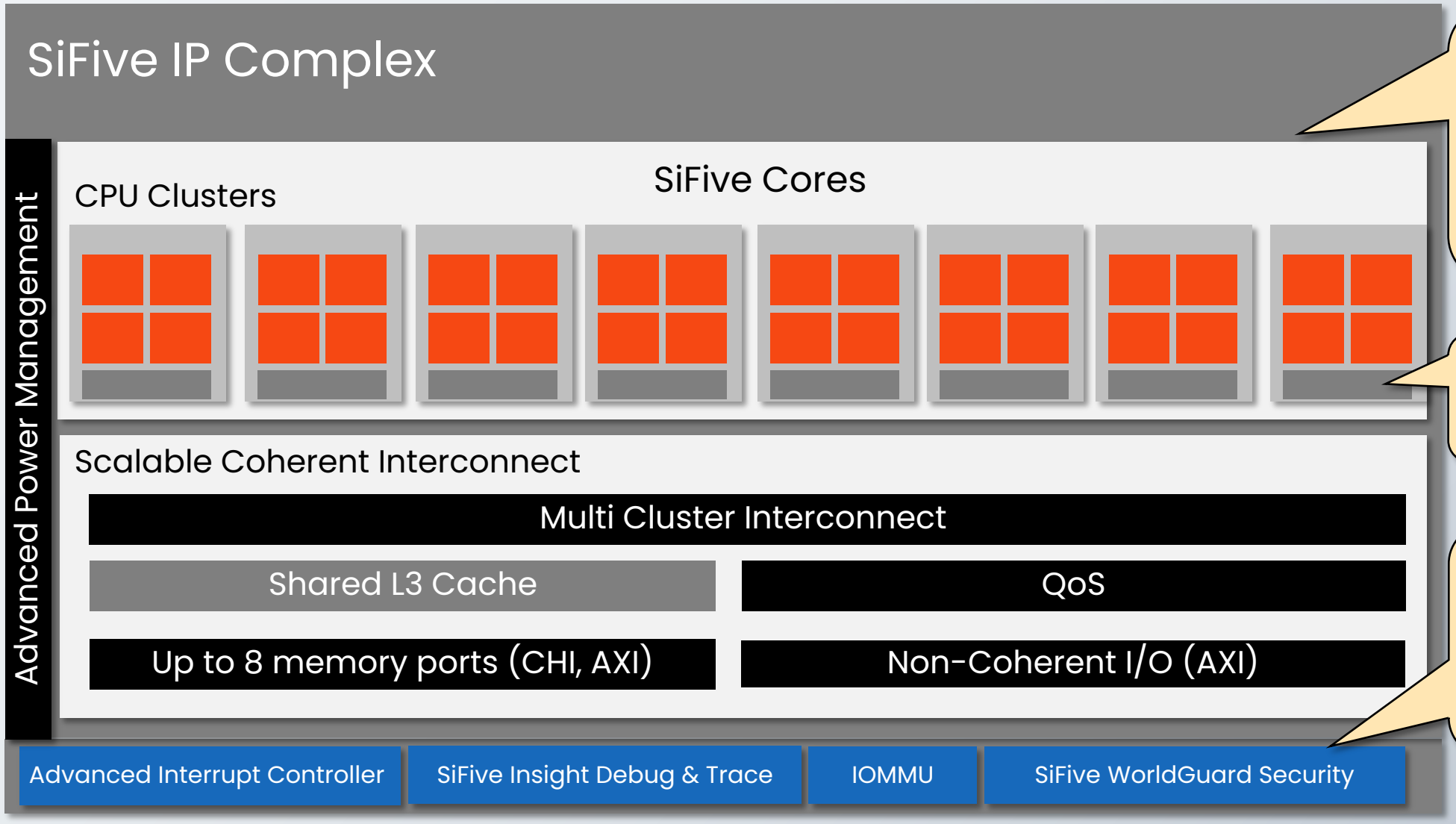
Automotive specific features

3rd generation OoO core

2022 2023 2024

Customer In-Silicon Dates

SiFive Provides Complete & Scalable Solutions

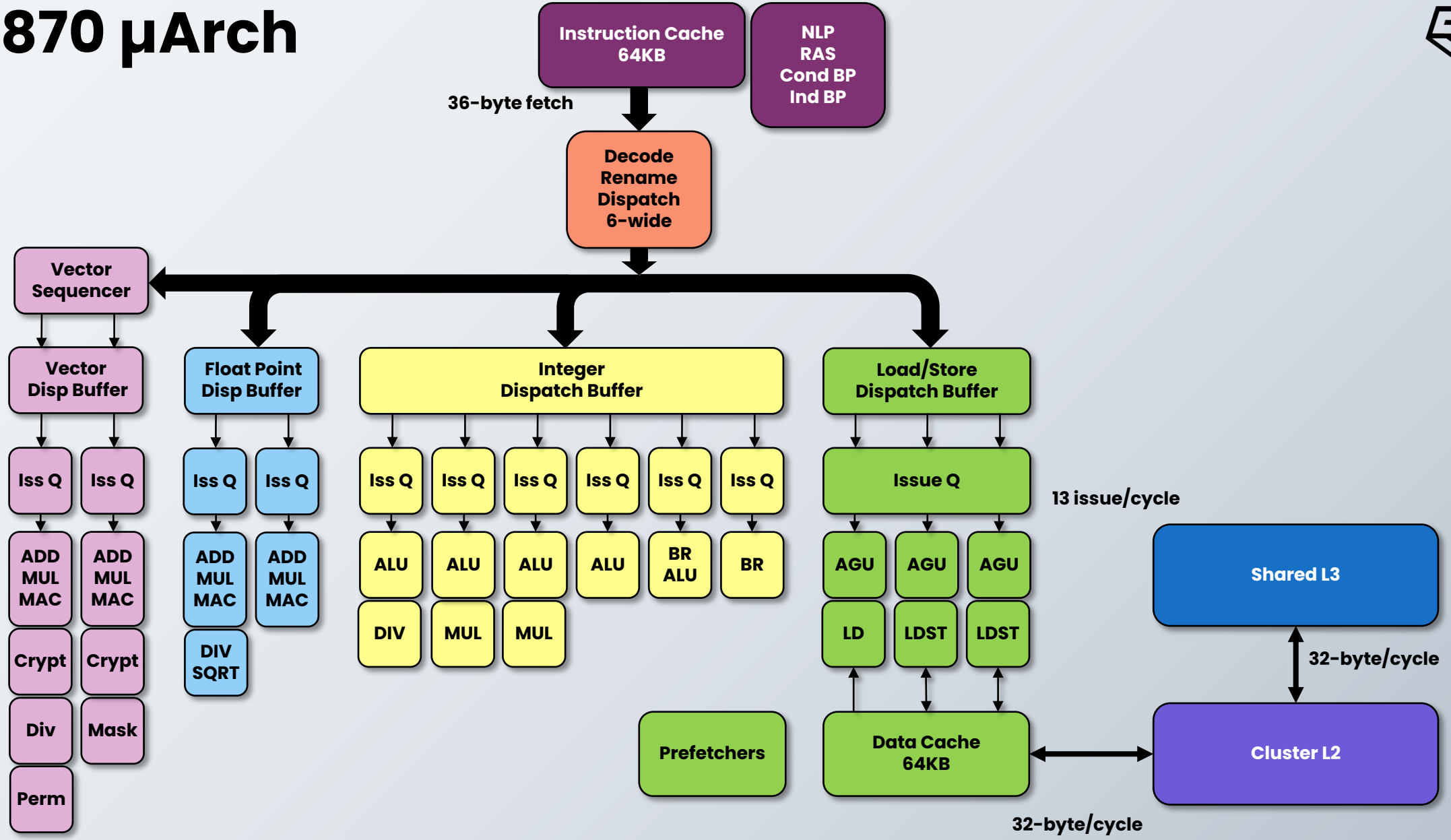


Scalable High-Performance & High-Efficiency Cores: P870, P670, & P470 (with selected Mix+Match)

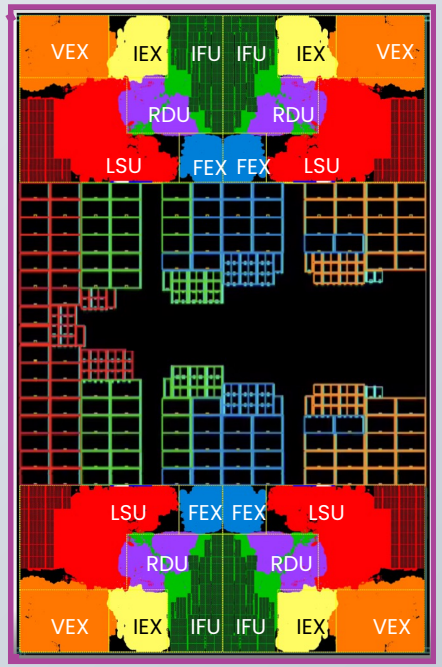
Shared Cluster L2 Cache

System IP to Enable Complete RISC-V SoC solutions

P870 µArch



Cluster topology with shared L2 cache and distributed L3 cache



P870 4-core cluster

Legend:

LSU - Load/Store Unit

IEX - Integer Execution Unit

FEX - Floating Point Execution Unit

VEX - Vector Execution Unit

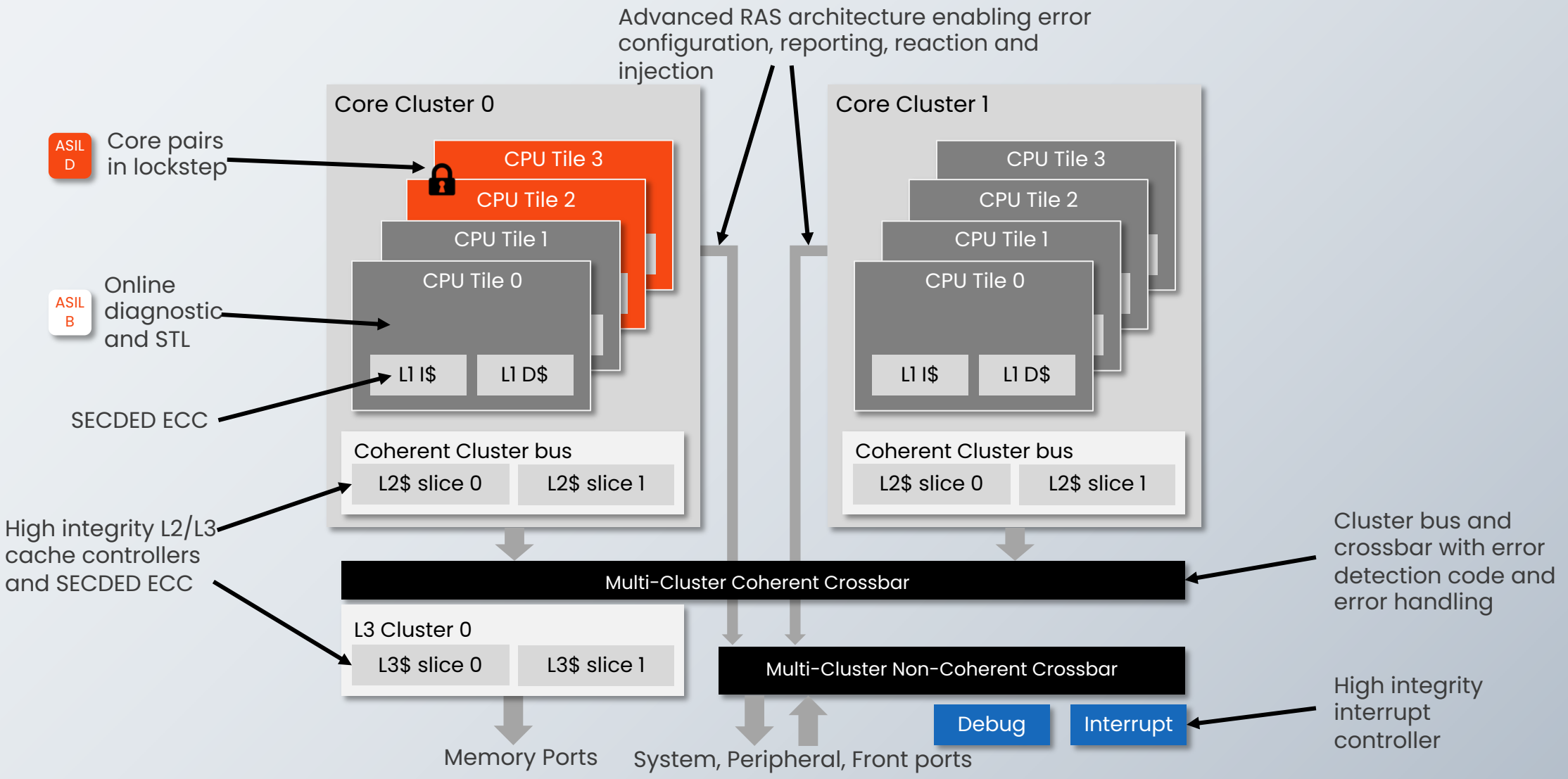
IFU - Instruction Fetch Unit

RDU - Rename/Dispatch Unit

P870 Consumer example platform

SiFive Advanced Debug & Interrupt
Interrupt Controller
Debug & Trace
SiFive CPU Clusters
Performance cluster
P870
P870
Shared L2$
High-efficiency cluster
P470
P470
P470
P470
Shared L2$
Always-On cluster
E6
Shared L3$
SiFive System IPs
IOMMU
WorldGuard gadgets

P870-A Functional safety features



SiFive Performance family relentless innovation

RVA20+

P550

RVA22/RVA23

P650/P670

P450/P470

RVA23

P870

More performance
Higher core count
Leading RISC-V feature deployment

P870-A

Automotive specific features

Napa

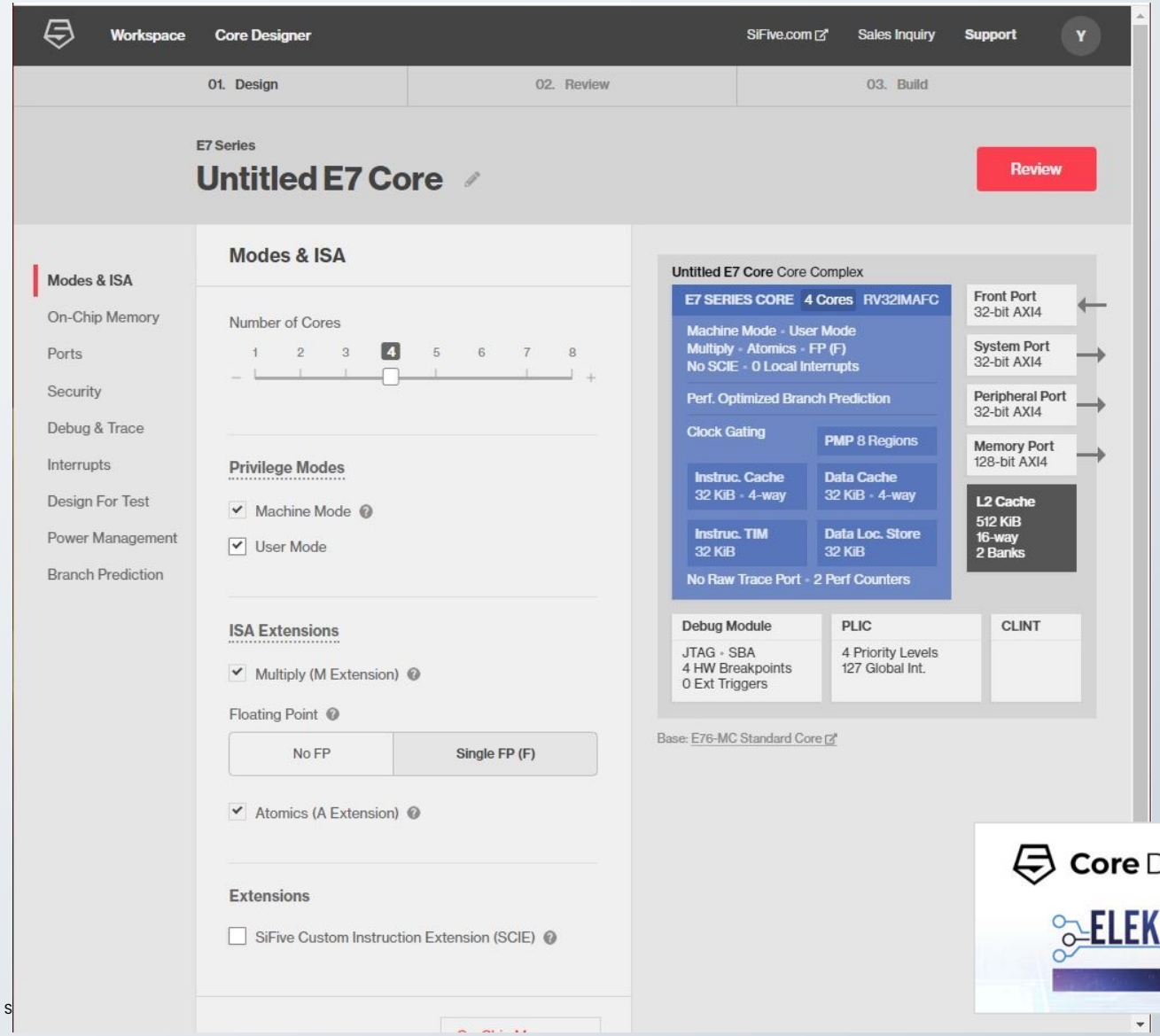
3rd generation OoO core

Customer In-Silicon Dates

2022 2023 2024

SiFive Core Designer

Optimize SiFive RISC-V Core IP for Your Application

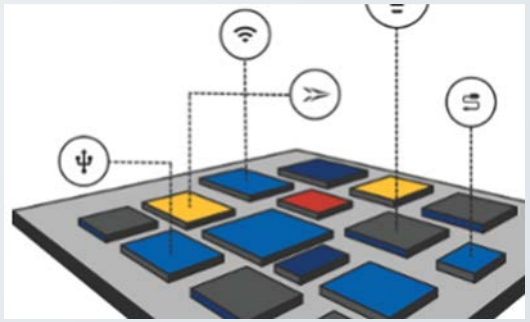


- SiFive Core Designer enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal
- **Variants** are generated with click of a button and are available from the Workspace
- **Variants** contain
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy integration into SiFive's SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC

Freedom Studio

Eclipse C/C++ Development Environment

- SiFive RISC-V Cross Compiler
- SiFive OpenOCD Debugger
- SEGGER J-LINK Debugger
- SiFive QEMU emulator
- SiFive Freedom E SDK software



Freedom Tools

SiFive

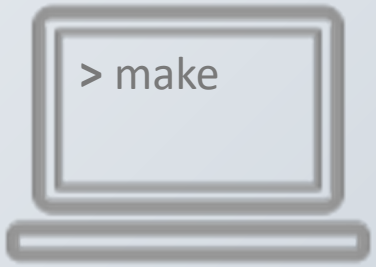
RISC-V development tools

- GNU Newlib Toolchain
- OpenOCD
- QEMU
- SDK Utilities
- Trace Decoder
- XC3SPROG

Freedom SDK for Metal

Bare metal software development

- Example programs
- Industry standard benchmarks
- Board support
- Metal library



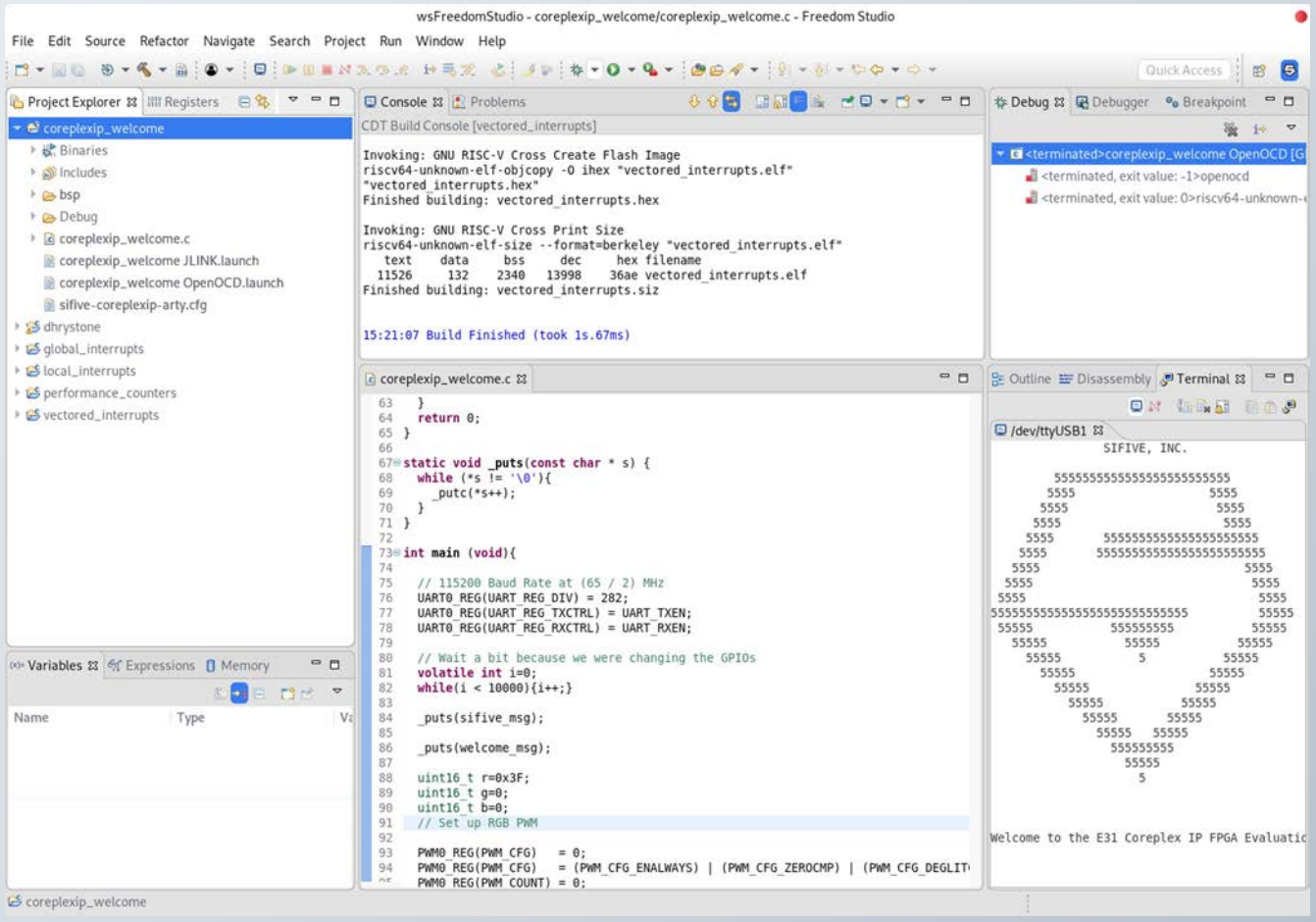
Freedom SDK for Unix

Embedded Linux software development

- Yocto / OpenEmbedded
- Board support
- Bootloaders
- Device tree binary
- Linux kernel images
- Disk images

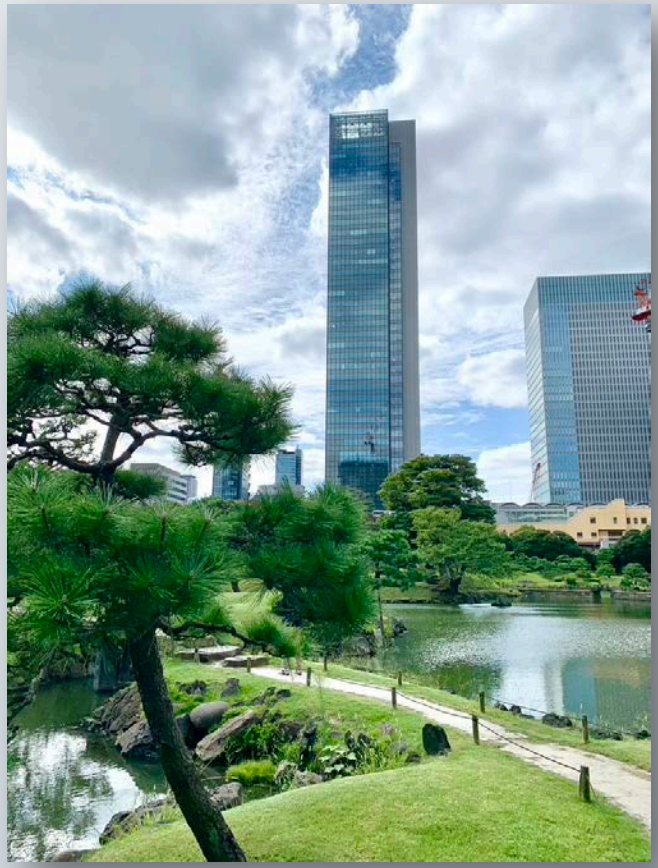
Build and Run the Software

- File - Import - DevKit Examples - Browse
- Select the zip that matches your core
- Select the desired examples and click Finish
- Control-B will build the entire workspace
- Run - Debug - OpenOCD starts a JTAG Debug Session and Loads the program



Contact us

We’d love to hear from you!
Get In Touch



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Thank you

www.sifive.com